

Non-Confidential Description - PSU No. 4112 **“Increased Efficiency in FPGA Arithmetic Operations”**

Keywords:

Multiplier, FPGA, look-up table, modified-booth recoding, multi-operand adder, signal processing, image processing

Inventors:

Eugene Walters

Links:

[Inventor Website](#)

[PCT Application](#)

Background

A field programmable gate array (FPGA) is used for computationally-intensive applications such as digital signal processing (DSP), video processing, image processing, and others. In these applications, multiplication is usually the dominant operation in terms of resource requirements, delay, and power consumption. Most modern FPGAs have embedded multipliers to deal with this issue, sometimes several thousand on one device. Unlike FPGA multipliers, LUT-based multipliers can be placed anywhere, their operands can be any size or type, and their number is limited only by the size of the FPGA. LUT-based multipliers are also used with embedded multipliers to make larger multipliers.

Invention Description

Since LUT-based multipliers are a low-level building block that is important to many applications. This invention is a drop-in replacement for general-purpose or constant-coefficient multipliers in existing designs that would significantly improve many applications with little extra engineering effort. The disclosed LUT-based multipliers use significantly fewer resources (LUTs) and are faster than any known competing designs. They have been compared to Xilinx LogiCORE IP multipliers and use 32% to 52% fewer LUTs, have up to 22% less delay, and can increase throughput by up to 2.5 times for a fixed area on the FPGA. These advantages are gained through algorithm improvements and efficient usage of the 6-input LUT.

Advantages/Applications

- Use 32% - 52% fewer LUTs
- Have up to 22% less delay
- Increase throughput up to 2.5 times for a fixed area on the FPGA
- Serves as a drop-in replacement for general-purpose and constant-coefficient multipliers
- Ideal for deeply pipelined, high frequency signal and image processing

Contact: Bradley A. Swope
Sr. Technology Licensing Officer
The Pennsylvania State University

Phone: (814) 863-5987
Fax: (814) 865-3591
E-mail: bradswope@psu.edu

June-15



Technology Available for Licensing
Office of Technology Management - The Pennsylvania State Univ.
113 Technology Center, University Park, PA 16802
814.865.6277 phone - 814.865.3591 fax

Contact: Bradley A. Swope
Sr. Technology Licensing Officer
The Pennsylvania State University

Phone: (814) 863-5987
Fax: (814) 865-3591
E-mail: bradswope@psu.edu

June-15